

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Andrew Horch et al.)	Examiner: Unknown
)	
Serial No.:)	Group Art Unit: Unknown
)	
Filed: herewith)	
)	
For: Recessed Thyristor Control Port)	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:


Listed on the attached Form PTO-1449 is information known to applicant. Each reference cited herein was previously cited in parent applications and a copy of each reference was provided to the Examiner, or cited by the Examiner in an Office Action. No additional copies of the references are being submitted with this paper, but will be furnished upon the Examiner's request.

Applicants respectfully request that the listed information be considered by the Examiner and be made of record in the above-identified application. If form PTO-1449 is enclosed, the Examiner is requested to initial and return it in accordance with MPEP 609.

This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in section 1.56.

Respectfully submitted,

Date: December 5, 2003


Hark C. Chan (Reg. No. 35,477)

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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	
Filing Date	
First Named Inventor	Andy Horch
Art Unit	
Examiner Name	
Attorney Docket Number	C016-D-1

Sheet 1 of 2

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 6,229,161	5-8-2001	Nemati et al.	
		US- 6,104,045	8-15-2000	Forbes et al.	
		US- 6,128,216	6-27-2000	Amerasekera et al.	
		US- 6,081,002	5-1-2001	Noble, Jr. et al.	
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FOREIGN PATENT DOCUMENTS

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	
				Filing Date	
				First Named Inventor	Andrew Horch
				Art Unit	
Examiner Name					
Sheet	2	of	2	Attorney Docket Number	C016-D-1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		K. DeMeyer, S. Kubicek and H. van Meer, Raised Source/Drains with Disposable Spacers for sub 100 nm CMOS Technologies, Extended Abstracts of International Workshop on Junction Technology 2001.	
		Mark Rodder and D. Yeakley, Raised Source/Drain MOSFET with Dual Sidewall Spacers, IEEE Electron Device Letters, Vol. 12, No. 3, March 1991	
		Yang-Kyu Choi, Daewon Ha, Tsu-Jae King and Chenming Hu, Nanoscale Ultrathin PMOSFETs with Raised Selective Germanium Source/Drain, IEEE Electron Device Letters, Vol. 22, No. 9, September 2001.	
		N. Lindert, Y. K. Choi, L. Chang, E. Anderson, W. C. Lee, T. J. King, J. Bokor, and C. Hu, Quasi-Planar FinFETs with Selectively Grown Germanium Raised Source/Drain, 2001 IEEE International SOI Conference, 10/2001	
		T. Ohguro, H. Naruse, H. Sugaya, S. Nakamura, E. Morifuji, H. Kimijima, T. Yoshitomi, T. Morimoto, H.S. Momose, Y. Katsumata, and H. Iwai, High Performance RF Characteristics of Raised Gate/Source/Drain CMOS with Co Salicide, 1998 Symposium on VLSI Technology Digest of Technical Papers	
		Hsiang-Jen Huang, Kun-Ming Chen, Tiao-Yuan Huang, Tien-Sheng Chao, Guo-Wei Huang, Chao-Hsin Chien, and Chun-Yen Chang, Improved Low Temperature Characteristics of P-Channel MOSFETs with Si1-xGex Raised Source and Drain, IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001	
		Plummer, James, D. and Scharf, Brad W., Insulated-Gate Planar Thyristors, I-Structure and Basic Operation, pp. 380-386	
		Stanley Wolf Ph.D. and Richard N. Tauber Ph.D., Silicon Processing for the VLSI Era, Vol. 1, 1986, page 285-286	

Examiner Signature		Date Considered	
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